FPGA board irradiation tests - possibilities

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Introduction

The goal of this experiment is to get known FPGA chip and whole electronic systems behaviour in the accelerator tunnel. Tests have to show number and structure of errors appeared in the chip and the system. The next step will be developing of proper shields for use in Tesla experiment to prevent observed problems.

FPGA architecture

Overview

FPGA stands for Field Programmable Gate Array. That's the chip, which is programmed by user to perform the desired functionallity. There are many possibilities of programming (types of FPGA):

- Antifuse technology - programmed only once
- Flash based - programmable several times
- SRAM based - programmable dynamically

The last possibility is dominating technology. It allows very fast, unlimited in system reprogramming. This type of FPGA chip is used for irradiation tests.

Architecture of FPGA from different vendors may differ but the main idea is almost the same. There will be shown on the example of Xilinx Spartan-IIE chip. FPGA architecure (picture 1) consists of:

- flexible, programmable Configurable Logic Blocks (CLB), which provide the functional elements for constructing logic
- programmable Input/Output Blocks (IOB), which provide the interface between the package pins and the internal logic
- Delay-Locked Loops (DLL) for clock distribution

- dedicated internal memory (Block RAM)
- varsatile multi-level interconnect structure

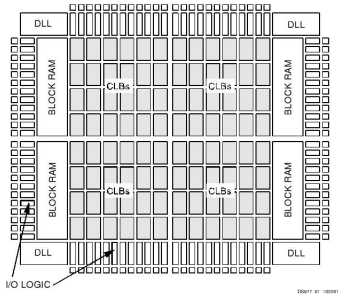

Figure 1: Basic Spartan-IIE Family FPGA Block Diagram

CLBs form the central logic structure with access to all support and rountings. IOBs are located around logic and memory elements for easy routing signals from and to chip. Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values must be loaded into the memory cells on power-up and can be reloaded to change function of the device, almost any time.

Configurable Logic Block

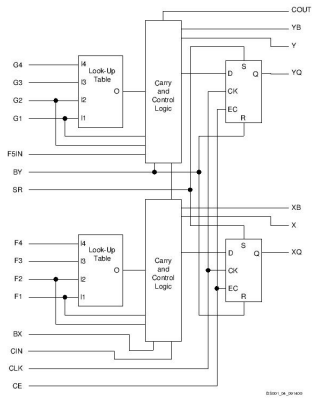

Figure 2: Spartan-IIE CLB Slice

The basic block of the CLB (picture 2) is Logic Cell (LC). Two LCs form slice and two slices form CLB. Each LC includes a 4-input function generator, carry logic and a storage element. The function generator is implemented as 4-input look-up table

(LUT). The storage element can be configured either as edge-triggered D-type flip-flop or as level-sensitive latch. The input of storage element can be output from function generator or direct slice input (bypass the function generator). Each slice has synchronous set and reset signals. These signals can be also independently inverted and can operate asynchronously. There is also additional multiplexer (F5) (picture 3) in each slice. It combines function generator outputs. This combination provides functions up to 9 inputs. Output multiplexer (F6) (picture 3) combines outputs of all 4 function generators in CLB. It provides functions up to 19 inputs. There is also carry logic block in each slice, which provides fast arithmetic carry capability for high-speed arithmetic functions.

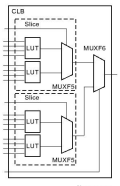

Figure 3: F5 and F6 multiplexers

Input/Output Block

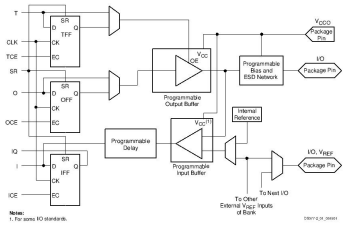

Figure 4: Spartan-IIE Input/Output Block

The IOB (picture 4) features inputs and outputs that support a wide variety of I/O signalling standards. It consists of:

- three registers, which can work either as edge-triggered D-type flip-flops or as level-sensitive latches
- programmable delay element in the input path, which eliminates pad-to-pad hold time
- two multiplexers to control output from FPGA

Each input can be configured to conform to any of the low-voltage signalling standards. Each output can be programmed for a wide range of low-voltage signalling standards.

Delay-Locked Loop

This block eliminates skew between the clock input pad and internal clock-input pins throughout the device. Additionaly delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input.

Block RAM

That's internal memory for use to storage data inside the chip. The word length can be configured by user.

Programmable Routing Matrix

The software automatically uses the best available routing based on user timing requirements. Local routing resources provide three types of connections:

- interconnections among the LUTs, flip-flops
- internal CLB feedback paths, beteen LUTs in the same CLB
- direct paths providing high-speed connections between horizontally adjecent CLBs

Configuration

This is the process by which the bitstream of a design is loaded into the internal configuration memory of FPGA. In experiment it's done by JTAG port.

Radiation induced errors in FPGA

The radiation can change the logic state of SRAM cell or flip-flop. Errors can give various effects:

- change of state of flip-flop results in false value stored in it
- change of state in SRAM cell in LUT results in permanent wrong answer of LUT
- change of state in memory describing interconnections results in wrong connections between internal structures of FPGA

The change of the logic state of one element caused by radiation is called Single Event Upset (SEU). There are two types of SEUs:

- static SEU - changes in configuration bits, changes functionality of FPGA
- dynamic SEU - change of bit stored in flip-flops, during one cycle period

Test board

In the experiment there is used Virtex II XC2V1000 Development Kit (picture 5) from Memec company.

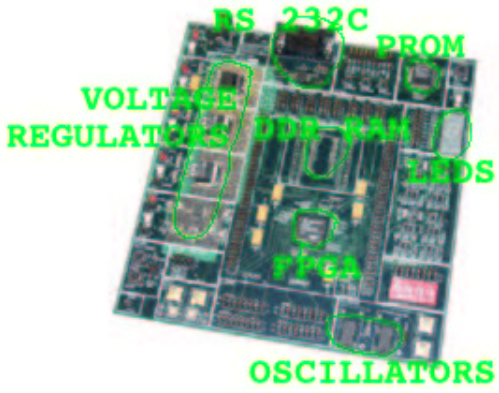

Figure 5: Virtex II XC2V1000 Development Kit

It utilizes:

- Virtex-II XC2V1000 device
- Toshiba TC59WM815BFT 16Mx16 DDR memory
- Xilinx XC18V04 ISP PROM
- two oscillators (24MHz and 100MHz)
- 7-segment LED display
- RS232C Interface
- 1.5, 1.8, 2.5, 3.3 voltage regulators

Planned experiments

Tests to be done during irradiation experiment of the FPGA board:

- test of FPGA configuration memory
- test of logic layer of the FPGA chip
- test of other components on the development board:
  - DDR memory
  - PROM memory
  - RS232C interface
  - buffers
  - oscillators
  - voltage regulators
- test of shieldings for electronic board

These tests will show not only FPGA chip sensivity to the radiation but bahviour of whole electronic system in irradiated environment.

Propositions of tests

In all experiments FPGA test board will be placed in the Linac II accelerator tunnel in various positions to get results of its sensivity on different radiation levels. The PC computer operating tests will stand in the Linac II Modulator Hall.

FPGA configuration memory

PC computer will perform readback function of FPGA configuration memory. FPGA will be programmed with some functionality and then the reading back of configuration data will be done. After comparing acquired configuration data with expected one number of differences will give number of static SEUs.

FPGA logic

FPGA test board will be programmed with big design, which utilizes as much resources of FPGA as it will be possible. It can be long shift register, which shifts data from its input to output. Input test vectors will be send by PC computer (or second FPGA board outside irradiation environment) and it will be compared with data from output. Differences will show errors - dynamic SEUs in FPGA. During this test the FPGA configuration memory test also will be performed. In case of any static errors in this memory the FPGA should be reprogrammed.

DDR memory

The FPGA will be programmed with DDR interface. It will perform also test of this memory and report all errors to the PC computer. During experiment PC computer will perform FPGA memory configuration test and in case of SEU errors in configuration it will reprogram FPGA. DDR memory will be refilled when too many errors will occure.

PROM memory

Test repeatable routine:

1. Loading configuration into PROM memory.
2. Programming FPGA from PROM memory.
3. Reading back data from FPGA configuration memory.
4. Comparing data acquired in step 3 with data with which the PROM was programmed (in step 1). Number of differences gives number of errors in PROM memory.
5. In case of many errors goto step 1, else goto step 2.

Other components on FPGA board

Other components like: voltage regulators, RS232C interface, oscillators seem to be less sensitive to the radiation. These elements will be tested passively during rest of experiments. In case of any problems the board will be tested outside the tunnel to know what part is broken.

Shields for electronic boards

According to data collected in LEDs, optical fibre and TLSs experiments there will be designed proper shieldings for neutron and gamma radiation. All proposed shields will be tested in accelerator tunnel with all tests mentioned before. The goal of this test is to design such shield for electronic board that gives the least number of errors.

References

[1] Trenz Electronic, "Tutorial: Introduction to FPGA Technology"

[2] Xilinx, "Spartan-IIE 1.8V FPGA Family: Functional Description"

[3] Xilinx, "Virtex-II Platform FPGAs: Detailed Description"

[4] Bunkowski, Kassammacov, Krolikowski, Kierzkowski, Kudla, Maenpaa, Rybka, Tuominen, Ungaro, Zabolotny, "Radiation tests of RPC trigger electronic components"