FPGA memory configuration irradiation tests - first results

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Introduction

The goal of this test is to measure only FPGA configuration memory sensivity to the radiation in accelerator tunnel. This is the first test, because according to the results of radiation tests done in Finland for CERN CMS experiment, large number of dynamic SEUs is not expected. The main idea is to use of readback function provided by Xilinx software.

Test system

The test system consists of:

- Virtex-II XC2V1000 Memec Development Kit - FPGA-based board
- PC computer, running appropriate software:
  - operation system: Windows 2000
  - Xilinx ISE WebPack 5.2
  - dedicated application written in Python language to perform tests

Programming is done by JTAG port. Because of long distance JTAG signals are distributed as LVDS signals.

Addditional elements

There are 3 TLD dosimeters and 5 LED diodes placed on the FPGA board. LED diodes will be evaluated, like in other experiment with LED diodes, to know neutron dose. There are two more TLD dosimeters (picture 1) to show changes of radiation in tunnel:

- one meter closer to converter (16,5 meters from it)
- one meter from the tunnel in the exit corridor

There is also CMOS camera, which aims on the Programmed Diode and LED Display on the Test Board and shows the status of chip.

FPGA board position

Test board with FPGA chip is placed in the tunnel, near the exit, as it's shown on the picture 1, 17.5 meters from electron-positron converter.

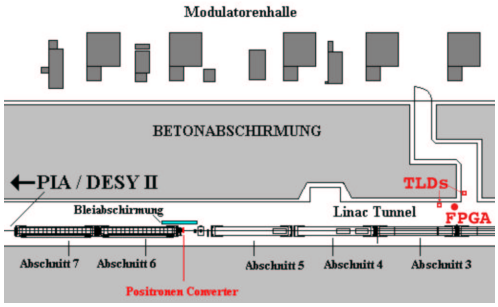

Figure 1: Linac II tunnel with FPGA Test Board inside

Test routine

Test performs writing and reading configuration from FPGA (picture 2). Programming is done every 1 hour. Reading is done every 2 minutes. After reading back acquired data from FPGA configuration memory is compared with data with which FPGA was programmed. Number of differences shows number of SEUs in FPGA configuration memory.

Results

The experiment was started on 22.08.2003 at 13:15. The Linac II beam energy was about 450 MeV. The beam current was very low and accelerator didn't work all the time.

Total number of all errors till the end of 26th August was 10. There were 4 SEUs in first verification after programming the FPGA. The rest was after some minutes (5, 9, 15, 19, 21, 29 - avarage: 16). Table 3 shows statistics of errors.

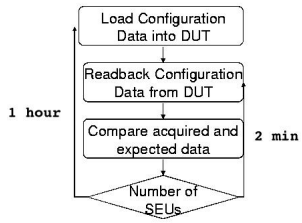

Figure 2: FPGA memory test routine (DUT - Device Under Test - FPGA test board)

Date	Number of errors	Number of errors after programming
22.08	1	1
23.08	4	0
24.08	2	1
25.08	2	1
26.08	1	1

Figure 3: Errors in FPGA configuration memory during first irradiation run of FPGA

There were no problems with power supplies and JTAG port.