Data Processing Board Design for CBM Experiment

Wojciech M. Zabołotny[a] and Grzegorz Kasprowicz[a]

[a]Institute of Electronic Systems, Warsaw University of Technology, ul. Nowowiejska 15/19, 00-665 Warszawa, Poland

ABSTRACT

This paper presents a concept of the Data Processing Boards for the Compressed Baryonic Matter (CBM) experiment. Described is the evolution of the concepts leading from the functional requirements of the control and readout systems of the CBM experiment to the design of prototype implementation of the DPB boards. The paper describes requirements on the board level and on the crate level. Finally it discusses the prototype design prepared for testing and verification of proposed solutions, and selection of the final implementation.

Keywords: Compressed Baryonic Matter, CBM, Readout, Front End Electronics, First Level Event Selector, Data Processing Boards, DPB, FPGA, MTCA.4, Etherbone

1. INTRODUCTION

The Compressed Baryonic Matter (CBM) experiment[1] at the FAIR facility in Darmstadt (Germany) is a new experiment, aimed on exploration of the QCD phase diagram in the region of high baryon densities during high-energy nucleus-nucleus collisions.[2] The CBM experiments will utilize multiple detectors including the Silicon Tracker (STS),[3] Muon Chamber (MUCH),[4] Transition Radiation Detector (TRD),[5] Micro Vertex Detector (MVD), Time of Flight Detector (TOF)[6] and Ring Imaging Cherenkov detector (RICH).[7] Each detector is connected to the Front End Electronic (FEE) boards, which provide it with necessary communication functionalities:

- Reception of the master clock and the timing information from the Timing and Flow Control (TFC) system.
- Transmission of the Flow Control related status to the TFC system.
- Reception of the synchronous commands from the TFC system.
- Reception of the setup and control commands from the Experiment Control System (ECS) and transmission of responses to those commands
- Transmission of received data to the First Level Event Selector (FLES),[8] which is the first stage of the data acquisition system.

The Front End Electronic boards are located near to detectors in an irradiated area. In the currently proposed setup, in most CBM detectors, the front end boards will be equipped with so called e-port[9] interfaces, and will be connected to the Readout Boards (ROB), which uses the radiation hard GBTX ASIC.[10] The GBT[11] technology was developed in CERN for upgrade of the LHC based experiments.[12] The GBTX chip uses 4.8 Gb/s bidirectional optical link for communication with TFC, ECS and FLES systems located outside the irradiated area. At the the FEE side it allows to establish deterministic latency bidirectional communication with the e-ports connected via SPI-like e-links,[9] transmitting up to 120 bits of information every 25 ns.

Transmission of the acquired data from ROBs via 4.8 Gb/s links to the FLES (over the straight view distance of 350 m, while the length of the links due to limitations to fiber placement will be probably significantly higher) would be unjustified from the cost point of view.

As a solution, the Data Processing Boards (DPB) have been proposed, which are an additional layer, located near to the FEE boards, but outside the irradiated area. Due to this location the DPB layer may be based on standard, more complex electronic systems using the COTS FPGA or even embedded systems and faster optical links. The position of the proposed DPB layer in the CBM control and readout system is shown in Figure 1.

Further author information: (Send correspondence to W.M.Z.)
W.M.Z.: E-mail: wzab@ise.pw.edu.pl, Telephone: +48 22 234 7717

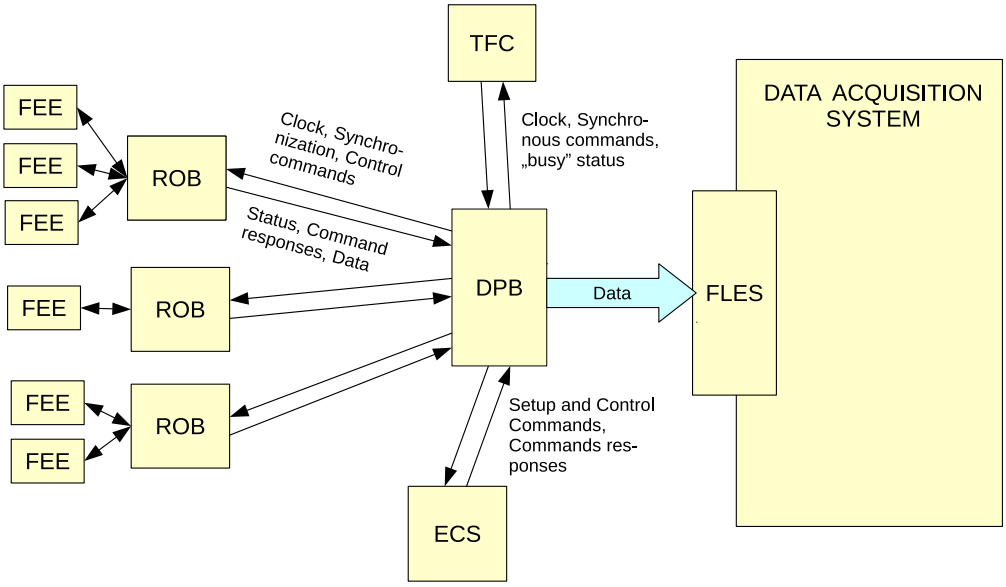

Figure 1. Position of the DPB layer in the CBM detector control and readout chain (based on a presentation prepared by Dr Walter Müller).

2. REQUIREMENTS FOR THE DPB LAYER

The previously described role of the DPB boards in the CBM experiment results in a series of requirements.

2.1 Reduction of links number

The main reason to use DPB is to allow aggregation of the acquired data, to reduce the number of optical links. To achieve that goal we must use the FLES links with higher speed than the FEE links. The concentration coefficient achievable in that way is simply the ratio between the link speeds, so the speed of the FLES links should be as high as possible. Unfortunately the cost of optical transceivers significantly increases with the link speed. Therefore the 10 Gb/s FLES links seem to be a reasonable choice, allowing to reduce the number of links by factor of 2.

Further reduction of the number of links may be achievable by reduction of amount of transmitted information. The information transmitted by FEE boards contains additional information (e.g. time markers, source identifiers etc.). When this information is aggregated and encapsulated in the format required by FLES, some of this fields become redundant and may be omitted.

The next method to reduce the amount of information which must be sent to the FLES, is to perform local processing of the data provided by the detectors, and to extract and transmit only important features. However applicability of that method is highly detector dependent. Therefore the DPB must be flexible enough to allow implementation of different data processing algorithms.

2.2 Transmission of the control commands between the ECS and FEE

The natural method to provide the communication between the ECS and the DPB layer is the computer network (e.g. the Ethernet based one). Therefore the DPB layer must provide translation between the network protocols and simple register access commands, which may be interpreted and performed by the FEE.

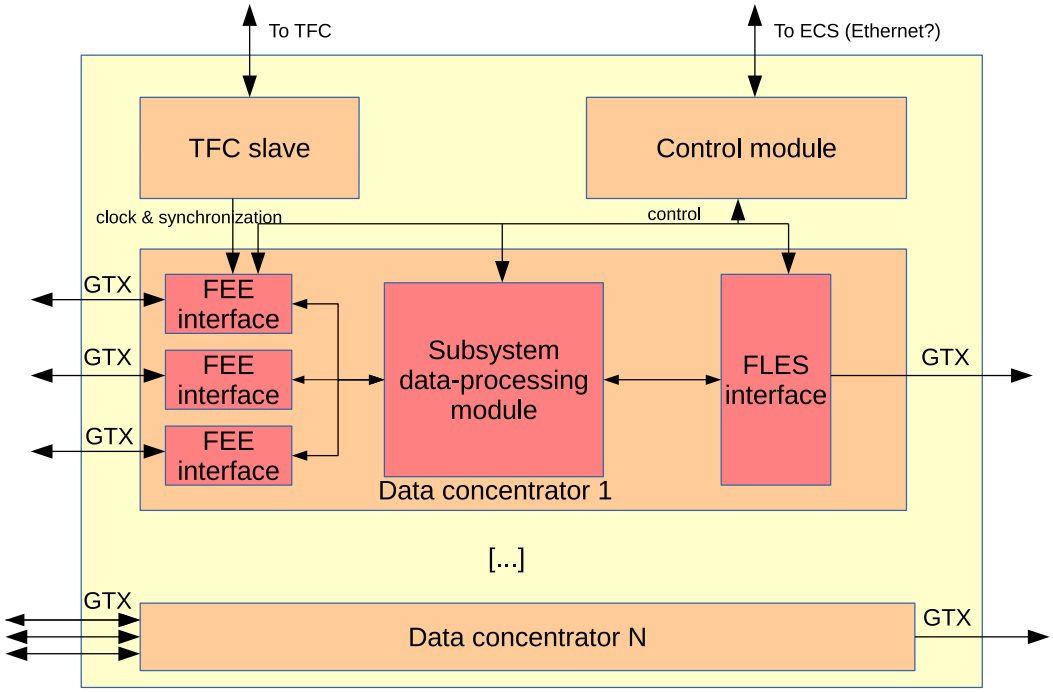

Figure 2. Functional blocks to be implemented in the DPB FPGA.

2.3 Transmission of the clock, timing and synchronous commands from TFC to FEE

The FEE layer must receive the master clock together with the synchronization information from DPB layer via communication link. It enforces use of deterministic latency communication protocol. It also requires that the clock used to drive the transmitters for FEE links must be recovered from the receiver clock from the TFC link. The DPB layer must also produce the "busy" status for the TFC system. To accomplish that each DPB board must monitor the occupancy of the connected FEE boards.

3. IMPLEMENTATION OF THE DPB LAYER

As the main function of the DPB is reception of data from multiple fast optical links, and transmission of processed data through another set of fast optical links, the natural platform for DPB implementation is the FPGA chip with multiple gigabit transceivers. Fortunately contemporary FPGA vendors offer reasonable number of gigabit transceivers even in FPGA chips with moderate prices. Good examples may be the Xilinx Series 7,[13] especially the Kintex-7 family.[14,15]

The layout of the internal logic to be implemented in the FPGA is shown in Figure 2

3.1 Implementation of the FEE communication block

The most difficult problem in implementation of the part of FPGA firmware related to the FEE communication was finding the IP cores able to establish deterministic latency communication with the FEE.

The first proposed solution was the CBMnet protocol and IP core[16,17] developed especially for that purpose for CBM.

However the later decision of the CBM collaboration to use the GBT technology (already described in the Introduction) allowed to use the GBT-FPGA[18] IP core dedicated for communication with the GBTX ASIC. The GBT-FPGA core is prepared for implementation in most modern FPGAs equipped with high speed gigabit transceivers (e.g. Xilinx - Virtex 6 & 7

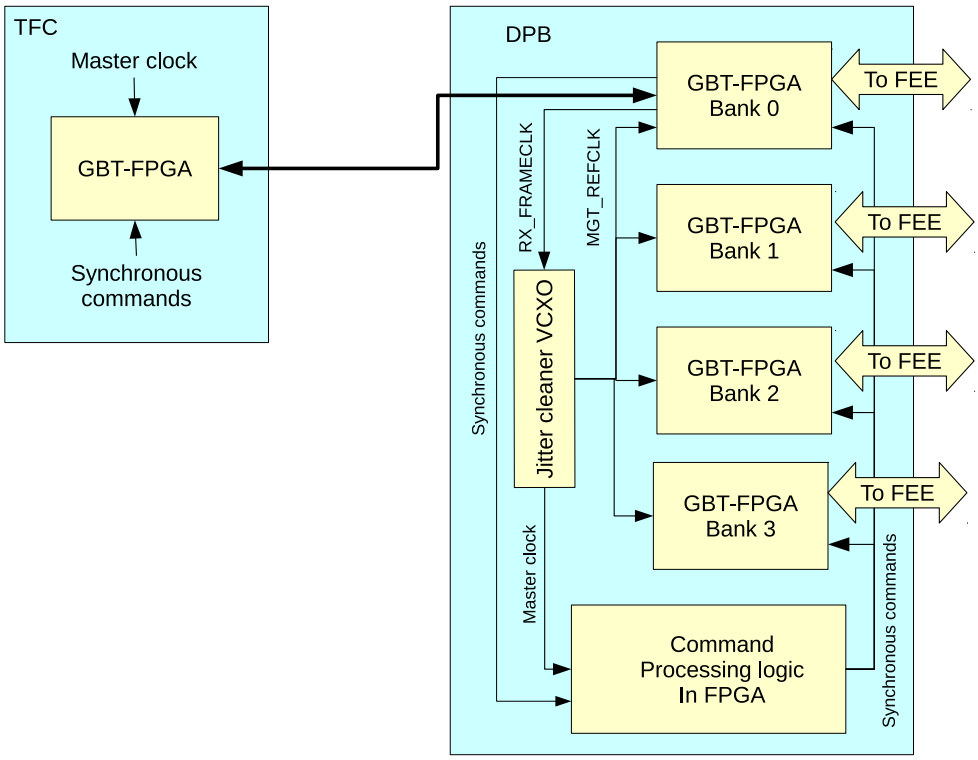

Figure 3. Usage of the GBT-FPGA in the autonomously working DPB board, with shown system for MGT clock recovery and cleaning. The most complex, GBT-FPGA based implementation of TFC system assumed.

and Kintex 7 or Altera - Cyclone V and Stratix V) The GBT-FPGA core may be configured to provide deterministic latency communication in both directions (deterministic latency may be selected for transmitter and/or receiver independently).

As it is mentioned in the Introduction, the GBT-FPGA core itself does not implement any special protocol for communication with FEE chips. Therefore it is necessary to develop such a protocol for particular subdetectors. Example of such protocol developed for the STS subdetector is described in Ref. 19.

3.2 Implementation of the TFC communication block

The timing and synchronization information may be transmitted from the TFC do DPB layer, using different technologies. One of them is the White Rabbit[20] technology. In such a case, the 125 MHz master clock will be distributed, together with the "Pulse Per Second" (PPS) signal. This 125 MHz clock must be later on converted to the 120 MHz clock, needed as the reference clock for GBT-FPGA links. This conversion may be achieved by conversion of the 125 MHz clock first to 5 MHz, and then to 120 MHz. The advantage of this solution is possibility to use low cost Ethernet equipment and cables. The synchronous commands in this solution should be sent in advance using the White Rabbit "critical data" technology, and scheduled for transmission to the FEE in the particular clock pulse.

Another solution, may be usage of GBT-FPGA cores to distribute clock and timing and to send synchronous commands. In this solution the master clock distributed by the TFC is available from the GBT-FPGA receiver, as the RX_FRAMECLK with frequency of 40 MHz. Additionally the GBT-FPGA receiver delivers the RX_WORDCLK clocks with frequency of 120 MHz, which after the jitter cleaning may be used as the reference clock (MGT_REFCLK) for GBT-FPGA links communicating with the FEE boards (see Figure 3).

The jitter cleaner system may be implemented in two different ways:

- With the standard PLL clock distribution IC with external VCXO. The clock recovered from GTX receiver (RX_FRAMECLK) is fed via a general purpose IO to the reference input of the PLL circuit. The PLL output provides the jitter-cleaned clock which may be used as GTX reference. The disadvantage of this method is introduction of additional jitter during routing the recovered clock to the external pin of FPGA.
- With the hybrid PLL circuit, which consists of external VCXO tuned by serial DAC, controlled by digital filter and DDMTD (Digital Dual Mixer Time Difference) phase detector.[21] The phase detector compares recovered GTX receiver clock and VCXO clock. The error signal tunes the VCXO to keep the phase difference constant. Such approach is used in White Rabbit time synchronization system, deployed successfully in several applications using a few FPGA platforms.[20]

In this solution, transmission of synchronous commands with deterministic latency is provided by the GBT-FPGA core. The significant disadvantage of this approach is use of costly optical components. Additionally this solution provides very high communication bandwidth which will be not fully utilized.

Yet another approach may be to use the hierarchically organized TFC system in which the DPB boards will be connected via relatively short dedicated copper links to the TFC master. In such solution both master clock, the PPS and synchronous commands may be sent using the bi-phase or Manchester encoding. However the jitter cleaner will also be needed, as encoding introduces unacceptable jitter into the received clock.

3.3 Implementation of the FLES link

Transmission of the aggregated and preprocessed data to the FLES will be performed via GTX transceivers. As it is stated in Section 2.1, 10 Gb/s links should be used for that purpose. The FLES group has developed the FLES Interface Board (FLIB) and is developing the associated "FLES Detector Input Interface" IP core.

Another interesting option may be to use the 10GBASE-R Ethernet,[22] which allows to use the standard Network Interface Card (NIC) in the FLES. It could be tempting to use the standard TCP/IP protocol to transmit acquired data to the FLES, however implementation of the standard TCP/IP stack working efficiently with 10 Gb/s link in the FPGA consumes a lot of resources. There exists a lightweight implementation of reduced TCP/IP protocol[23] developed for the CMS experiment Data Acquisition System, however sources of this solution are not widely available. Another possibility is to develop a dedicated network protocol, oriented on reliable transfer of data from FPGA to to FLES. The early version of such protocol for reliable transmission of measurement data from the FPGA with small resources consumption has been developed and is publicly available.[24]

The disadvantage of using the 10GBASE-R Ethernet technology is the fact, that it requires bidirectional links. In the FLES link the bandwidth needed for transmission of data from DPB to FLES will be much higher, than the bandwidth needed to transmit acknowledgements from FLES to DPB. If a protocol working with unidirectional links is used (e.g. the Xilinx Aurora 64B/66B[25]), then a single link from FLES to DPB may transmit acknowledgements for a few data links from DPB to FLES. Assuming, that a single DPB board supports 4 FLES links, implementation of the Ethernet base solution would require 8 fibers (4 in each direction), while implementation based on unidirectional links would require only 5 fibers (4 from DPB to FLES, and 1 from FLES to DPB).

3.4 Implementation of the data processing module

As it has been described in section 2.1, the data processing will heavily depend on the detector to which the particular DPB will be connected. For some detectors local processing of data and extraction of significant features can be done, leading to significant reduction of data, while for other detectors, the only processing may be associated with the time sorting of incoming data and encapsulation in the FLES requested "microslice"[26] format. Therefore on the current stage, the DPB firmware will only implement the framework for the detector specific data processing. The proposed framework will contain services such as:

- Reception and unpacking of data from the input GBT links
- Time sorting of data (the versatile sorter has been developed[27] has been developed, but in many cases a simplified methods, based on the knowledge about possible data records ordering, may be applied)

- Encapsulation of the processed data in the microslice containers
- Sending of the data to the output link

An example of the subdetector requiring significant data processing in the DPB layer is the TRD detector,[28] using the SPADIC ASIC.[29]

3.5 Implementation of the slow control module

The slow control will be associated with the access to the internal registers of the DPB FPGA. The standard open and extensible solution for communication with subsystems implemented in FPGAs is the Wishbone bus.[30,31] Because the preferred option to implement the slow control is a standard computer network, we can use an extension allowing to control the Wishbone bus remotely, via Ethernet network – the Etherbone core.[32–34]

4. SELECTION OF THE CRATE TECHNOLOGY FOR DPB BOARD

Even though possibility to have a single, autonomously working DPB board is highly desirable during the development, in the final system the DPB boards should be placed in a crate allowing to provide the mechanical support, power supply and connectivity. Additionally organizing the DPB boards in crates allows to avoid implementing of some necessary services in each board individually, as it is described later.

For many years the standard crate solution for the HEP measurement systems was VME,[35] however this technology, is generally outdated and not recommended for new designs. The most powerful crate technology for the measurement and data processing systems is probably the ATCA (Advanced Telecommunications Computing Architecture).[36] Unfortunately this technology is too expensive for our purpose. The cheaper solution widely used in different HEP experiments is the MictroTCA (MTCA),[37,38] especially in the version MTCA.4 (MicroTCA for Physics).[39,40] Therefore finally the MTCA.4 crate was selected for implementation of the DPB infrastructure.

4.1 Communication between the TFC system and the DPB crate

The DPB boards will be built as the Advanced Mezzanine Cards (AMC).[41] The DPB crate may contain up to 12 AMCs. To simplify the design, only one of those AMCs will receive the clock, timing and synchronous commands from the TFC system, and send the "busy" status to the TFC (it will be the "TFC slave" board). Preferably this board should also work as a standard DPB board, however it depends on a final choice of the TFC technology. If a solution consuming significant amount of FPGA resources will be chosen, the "TFC slave" will offer only a limited DPB functionality.

The master clock and PPS signal will be distributed by the MTCA.4 backplane using the MCH crossbar. The 120 MHz "Master clock" may be distributed as TCLKA, and the PPS may be distributed as TCLKB respectively. Another TFC related signals may be distributed via 8 M-LVDS lines available as ports 17-20 in the MTCA.4 backplane.

To implement the Flow Control, it is necessary, that the DPB board may signal the "busy" state. In fact it is important to state in the real time, that at least on of the DPB boards is "busy" (more detailed check of their statuses may be done via the slow control interface). This allows to collect the "busy" information using the single M-LVDS line, connected to the M-LVDS type 2 receiver located in the board implementing the "TFC slave" block.

The remaining 7 M-LVDS lines may be used to transmit synchronous commands.

4.2 Implementation of the slow control in the DPB crate

The MicroTCA Carrier Hub (MCH) which is the part of the MTCA.4 crate distributes the 1 Gb/s Ethernet to all AMCs board. This allows using it for slow control via the Etherbone core, as described in section 3.5. The disadvantage of this approach is consumption of one GTX transceiver in each DPB card. There are several options that save the GTX resources:

- Usage of MLVDS links. Each AMC board has unique geographical address that can be used to implement simple communication protocol. The board with "TFC slave" block then could be used as a communication bridge between Ethernet and MLVDS. Simple serial protocol could be implemented using even single MLVDS lane. Since the MLVDS can work easily at 80 MHz, achievable data rate seems to be sufficient for slow control.

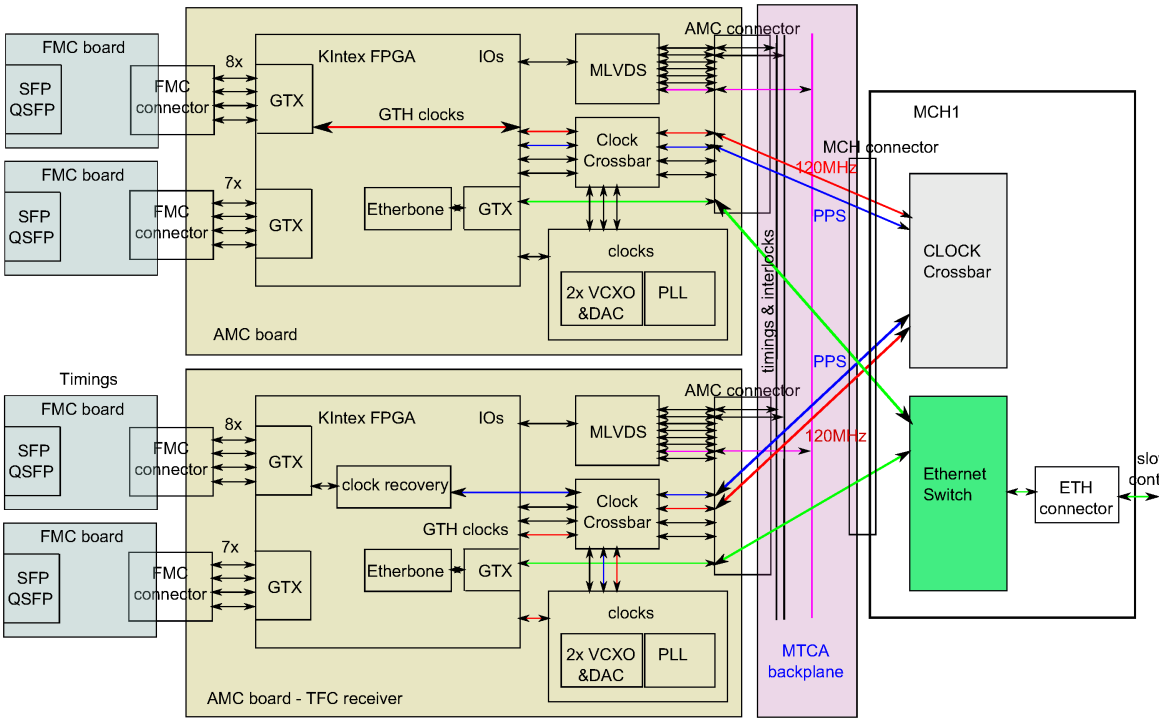

Figure 4. The prototype DPB board in the MTCA.4 crate with example of signals' routing.

- One can add external SER-DES chip (i.e. TLK3131) connected to PORT0/1 from one side and to some IOs of FPGA on the other side. Then, Etherbone IP core can talk directly with the SERDES using RGMII port.
- Another option is to use RTM connectors to implement point-to-point solution based on LVDS IOs of FPGA. This would require dedicated cabling and custom RTM boards but gives great flexibility. In the case where RTMs are used as holders for optical transceivers, such solution would not add significant cost to the system. In this concept, The board with "TFC slave" block would receive commands over 1 Gb/s Ethernet and would have to implement a bridge between the Etherbone and e.g. the Wishbone Serializer[42] cores. This allows control of the DPB cards via high speed serial connection using standard SERDES[43] blocks available in the Xilinx 7 Series FPGAs.

4.3 Implementation of the FEE and FLES connectivity in the DPB crate

There are several connectivity options for FEE and FLES. FLES links are based on single-mode optical transceivers that require 10Gbit/s bandwidth while FEE require multi-mode links running at 4.8Gbit/s. All these requirement can be covered by SFP or SFP+ optical transceivers respectively, but they are bulky and expensive. Moreover, providing that in the final solution we need more than 16 links, they will not fit to standard AMC panel, even with RTM extension card. Alternatively, QSFP transceivers can be used, they would give us up to 24 optical links per single AMC module (see Figure 5). Another, optional 24 links can be placed on the RTM board. Usage of the RTM board adds flexibility to the design since such board is relatively simple and low cost compared to complex and expensive FPGA AMC board. One can produce standard AMC boards with some common connectivity, and series of RTM boards with various optical links, for example mix of QSFPs, SFP+ and MiniPod[44] transceivers. Such a solution makes servicing easier and lowers the cost by reducing number of different expensive AMC boards. Another option is to use FPGA Mezzanine Cards (FMC) which would host optical transceivers. But they are much more constrained due to small size of the board. Single FMC can hold up to 4 SFP+ or 2 QSFP modules. Up to 2 FMCs can be used on single AMC.

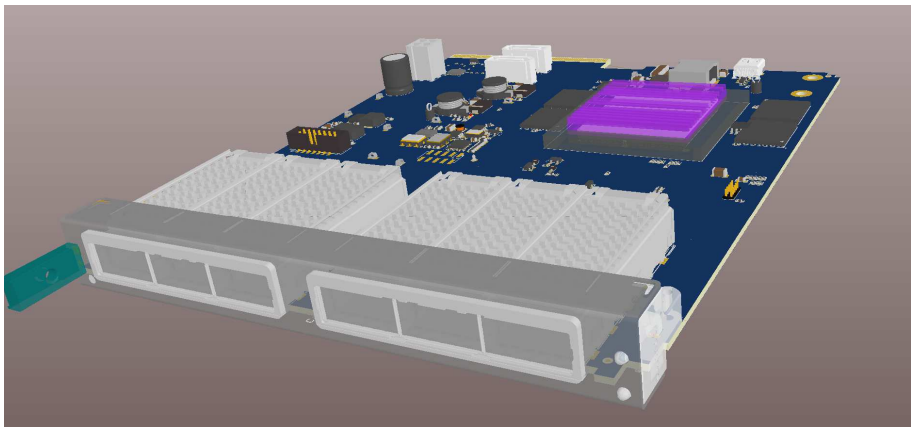

Figure 5. Drawing of AMC board with 24 optical links using QSFP transceivers

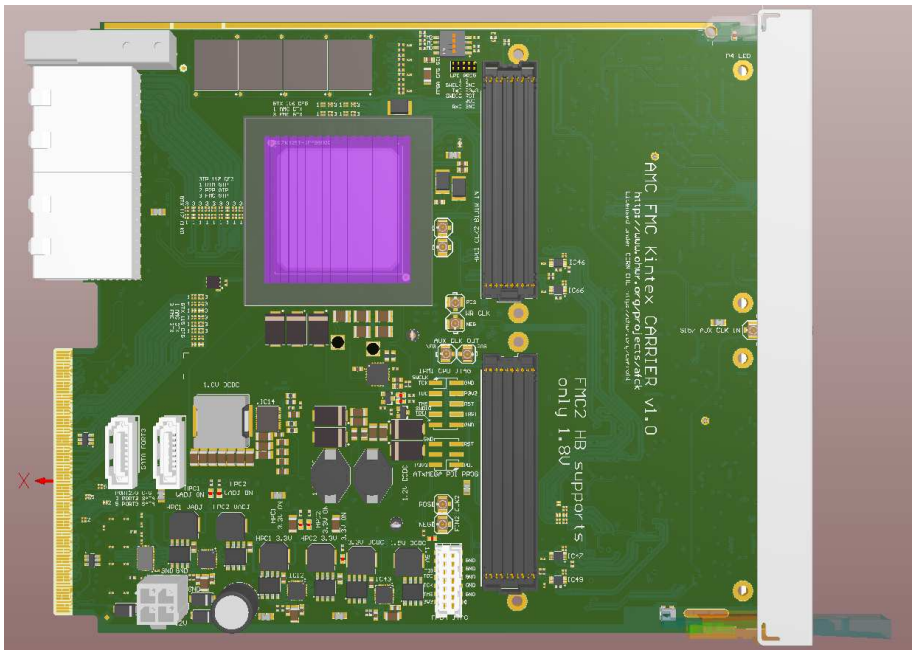

Figure 6. Drawing of the AMC FMC Carrier with Kintex 7 FPGA (AFCK).

5. PROTOTYPE OF THE DPB BOARD

The hardware implementation of the DPB board has been designed, and is available in the Open Hardware repository, as the AMC FMC Carrier Kintex (AFCK)[45] project. It is a versatile board (see Figure 6) with several extension options thanks to 2 FMC sockets and RTM connector. All 16 GTX transceivers can be connected to FMC, AMC or RTM connectors by placing optional 0201 capacitors. The board can work stand-alone, without the MTCA crate, with only single +12V power supply required. It implements 8 MLVDS links that can be used as communication channel. If additional gigabit transceiver is required, it can be placed on FMC board, together with optical modules and connected to Port0/1 of the AMC connector using UFL jumpers. The board also has large (2GB), fast DDR3 memory that can be used to fully buffer two or more 10Gbit data streams. Versatile clock distribution circuit, based on 16x16 crossbar, together with numerous VCOs and VCXOs enables implementation of very complex clocking schemes. The AFCK can be also used to implement the "TFC slave" without hardware modifications.

5.1 Flexibility of the proposed design

The proposed implementation of the DPB prototype allows for further studies on optimal implementation. AFCK is a perfect candidate for the DPB prototype because optical connectivity is provided using low cost FMC boards allowing examination of several options. Use of AFCK board does not require investments in MTCA infrastructure (crate, controller, MCH, PSU). Changes of selected method for slow control communication does not require modification of the hardware part, since the board implements rich connectivity and clocking options.

6. CONCLUSIONS

The proposed design of the Data Processing Board prototype provides a hardware platform, allowing verification and testing of different solutions for required functionalities. The DPB prototypes may be used both standalone and in the MTCA crate. Placement of optical transceivers on simple FMC boards or on RTM modules allows to change the optical technology (MicroPOD, SFP+, QSFP) without designing of the new FPGA board. Final DPB solution may be based on the same concept as AFCK. Probably the only modification may be the replacement of FPGA with the next generation chip with increased number of gigabit transceivers.

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