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Selection of hardware platform for CBM Common Readout Interface

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ABSTRACT

The implementation of the CBM readout and DAQ chain is currently reconsidered. The proposed changes include replacement of two sets of FPGA-based boards with a single one: Common Readout Interface (CRI) board. The paper presents the analysis performed to select the optimal hardware platform for the CBM CRI, considering the cost and the number of input links serviced by a single board.

Keywords: FAIR, CBM, STS, readout chain, FPGA, DAQ

1. INTRODUCTION

The Compressed Baryonic Matter (CBM) experiment is being prepared at the new accelerator complex FAIR in Darmstadt. It is a fixed-target experiment aimed at analysis of high-energy nucleus collision, allowing exploration of the QCD phase diagram in the region of high baryon densities.^{1,2}

The products of collisions will be recorded by multiple particle detectors: Micro Vertex Detector (MVD), Silicon Tracking System (STS), Ring Imaging Cherenkov Detector (RICH), Muon Chamber (MUCH), Transition Radiation Detector (TRD), Time of Flight Detector (TOF), Projectile Spectator Detector (PSD).

The CBM readout chain is a distributed system connecting the detectors' Front End Boards (FEBs) with the Data Acquisition System. The electronics controlling the FEBs and receiving the measurement data will be placed in the service building, located in the vicinity of the detector. In the case of STS and MUCH readout, the FEBs will be equipped with STS/MUCH-XYTER2 (SMX2)³ ASICS, connected via copper links to the Common Readout Boards (CROBs).⁴ The CROBs implement a bridge between the SMX2 links and the GBT^{5,6} links used to transmit the control signals and the measurement data to the CBM service building. The data received from CROBs should be here concentrated and transmitted via long distance (ca.700 m) links to the First Level Event Selector (FLES) computer grid located in the computer center. The first proposed solution assumed using two different kinds of FPGA-based boards. The first of them - Data Processing Boards (DPB)^{7,8} should control FEBs and receive data via the GBT links, and send concentrated data via higher-speed long-distance optical links. The second kind of boards, the FLES Interface Boards (FLIB)^{9,10} will receive the data in the form of so called microslices, and transfer them via the PCIe interface into the memory of the FLES input nodes. Further processing, and building of so called time slices is performed by the InfiniBand interconnected FLES nodes. The block diagram of the readout chain based on that concept is shown in Fig. 1.

However, last years the tendency of using the computers in the earlier stages of data acquisition chain is visible. That approach has been proposed for new upgrades of the LHCb¹¹⁻¹³ and ATLAS¹⁴ detectors at LHC. Similar solution has also been proposed for CBM. In this approach,¹⁵ the functionalities of the DPB and FLIB are combined in a single PCIe board, further denoted as Common Readout Interface. That solution reduces the number of specialized boards and allows to use the standard high-speed network interfaces (e.g. InfiniBand) for long distance links. This approach also allows to better utilize the technological progress. The fact that the CRI boards must be designed and manufactured earlier, does not prevent us from using the newest achievable technology for the long-distance links. Usage of standard network adapters may also further reduce costs. The block diagram of the modified DAQ chain is shown in Fig. 2.

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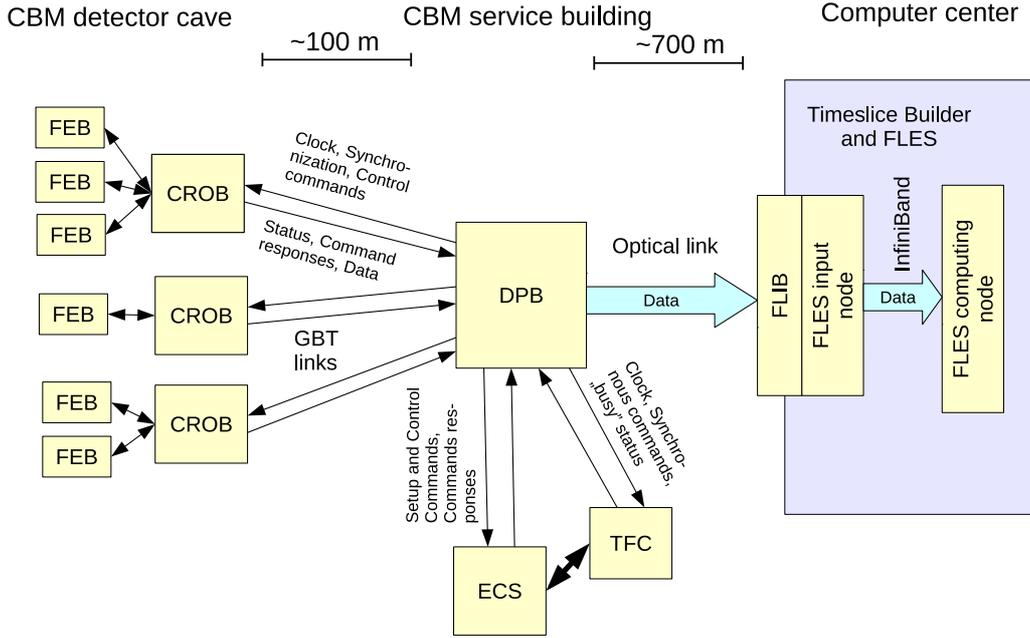


Figure 1: The first proposition of the CBM readout chain based on separate DPB and FLIB boards (based on [7]).

The design of the CRI boards, however, requires thorough checking of the available technology. The preliminary analyses were shortly described in [16].

2. REQUIREMENTS FOR THE CRI BOARD

The CRI board should be connected to the readout boards via GBT links. The readout board proposed for CBM⁴ provides three GBT links – one duplex and two simplex. Therefore to support N readout boards, the CRI should use $3 \cdot N$ multi-gigabit transceivers supporting the 4.8 Gb/s bitrate.

To transmit the concentrated data to the host PC, the CRI should also provide multi-gigabit transceivers able to implement the PCIe interface. Availability of the hardware PCIe core is also desired. Both leading FPGA vendors - Xilinx¹⁷ and Altera¹⁸ offer FPGAs with hardware implemented PCIe cores. However, Xilinx promises the hardware support for PCIe 4.0. Therefore the newest Xilinx family Ultrascale+^{19,20} was selected for further evaluation.

The most important criteria for selection of the right FPGA chip is the availability of the sufficient number of multi-gigabit transceivers. Of course it would be good to handle as many CROBs as possible with a single board, but there are certain limiting factors.

- Bandwidth
- Number of logical resources must be sufficient to concentrate the data

2.1 Available optical transceivers

Fitting multiple optical connections in a PCIe card may be a difficult task. Therefore miniature multichannel transceivers are needed. A quick search shows the following options (prices taken from Octopart²¹):

- QSFP+: Finisar FTL410QD2C²² with approximate price of \$300 for 4 duplex channels.
- 12-channel - Foxconn MiniPOD²³ modules with the approximate price of \$360 for simplex channels (either Tx or Rx).

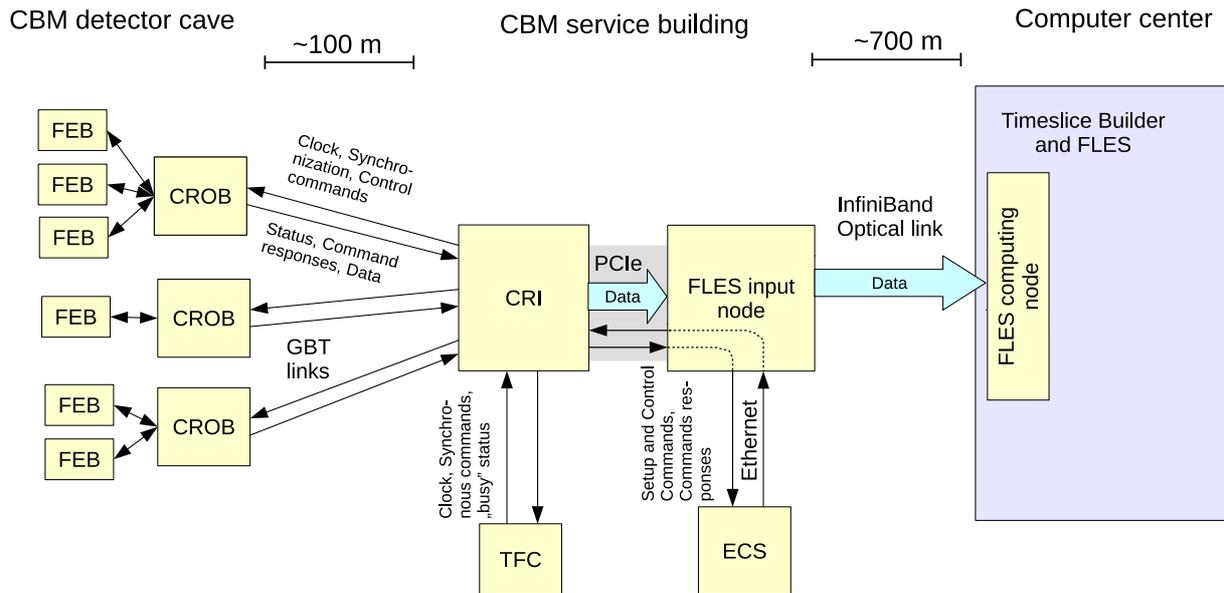


Figure 2: Proposition of the modified readout chain with CRI (based on [15]).

- 12-channel - Foxconn MicroPOD²⁴ modules with the approximate price of \$130 for 12 Tx channels and \$280 for 12 Rx channels.
- 24-channel - Finisar FBOTD10SL1C00²⁵ with the approximate price of \$860 for 24 duplex channels. The RX only FB RTP10SL1C00 modules are also available.

It seems that the best cost per channel may be achieved with the 12-channel MicroPOD modules. The smallest configurations with a reasonable utilization of optical channels are the following:

- With two 12-channel receivers and one 12-channel transmitter, we can connect 8 CROBs to a single CRI. In this case, we waste 4 transmit channels (may be used as spares).
- With three 12-channel receivers and one 12-channel transmitter, we can connect 12 CROBs to a single CRI. In this case, we fully utilize optical channels.

2.2 Required PCIe bandwidth

The number of handled CROBs also defines the required PCIe bandwidth. In the pessimistic approach, we may consider that the required PCIe bandwidth will be just the sum of data bandwidth from all connected GBT links. In the "wide bus" mode used in the STS readout, each GBT link may deliver 4.48 Gb/s of data. That gives 13.44 Gb/s of data for each CROB, resulting in 108 Gb/s for 8 CROBs and 162 Gb/s for 12 CROBs.

The optimistic approach considers the format of data delivered by the STS FEE.²⁶ Each SMX2 link delivers up to 9.41 Mhits/s. In each hit, 20 bits of information cannot be aggregated. Assuming, that each CROB board may service up to 40 SMX2 links, we get the data bandwidth of 7.53 Gb/s from each CROB and finally 60.22 Gb/s for 8 CROBs and 90.34 Gb/s for 12 CROBs.

The PCIe 3.0 or 3.1 offers us 7.877 Gbit/s per lane, and UltraScale+ devices may use up to 16 lanes. So assuming the pessimistic assessment, we need 16 lanes for 8 CROBs (bandwidth 126 Gb/s - margin of 14%) and two links each with 16 lanes for 12 CROBs (bandwidth of 252 Gb/s - margin of 36%). Assuming the optimistic assessment, a single link with

8 lanes should be sufficient for 8 CROBs (bandwidth of 63 Gb/s) but the margin of 4% is probably too low, and therefore anyway the 16-lanes link will be needed. The same link will be needed in case of 12 CROBs (margin of 28%).

The PCIe 4.0 offers us 15.752 Gb/s per lane, and UltraScale+ devices may use up to 8 lanes. The similar analysis gives us for pessimistic assessment one 8-lanes link for 8 CROBs and two 8-lanes links for 12 CROBs, and for optimistic assessment - one 8-lanes link both for 8 and 12 CROBs.

The above results are summarized in table 1 and in table 2.

Table 1: Required number of multi-gigabit transceivers for different interfaces depending on bandwidth assessment and PCIe version.

# CROBs	# GBTs	#lanes PCIe 3		#lanes PCIe 4	
		opt.	pess.	opt.	pess.
8 CROBs	24	16	16	8	8
12 CROBs	36	16	32	8	16

Table 2: The total required number of multi-gigabit transceivers depending on bandwidth assessment and PCIe version. One multi-gigabit transceiver is added for a possible TFC connection.

# CROBs	PCIe 3		PCIe 4	
	opt.	pess.	opt.	pess.
8 CROBs	41	41	33	33
12 CROBs	53	69	45	53

The results of the comparison of the above requirements with the available Ultrascale+ chips¹⁹ are shown in table 3. The Virtex chips were avoided to keep the cost of the CRI board as low as possible.

Table 3: Available chips and their resources. Prepared basing on [19]. Example prices found on Octopart.²¹ Prices for chips in speedgrade “1” and temperature range “E”, except XCKUP15P in enclosure FFVA 1760*, where only the price for speedgrade “L2” was available. Assuming the same price ratio between “1” and “L2” parts as in the case of XCKUP15P in FFVE1760 enclosure, we may estimate the price of “1” speedgrade at ca. \$5000.

	KU11P	KU15P		ZU11EG	ZU17EG		ZU19EG	
System Logic Cells	653,100	1,143,450		653,100	926,194		1,143,450	
Block RAM Blocks	600	984		600	796		984	
UltraRAM Blocks	80	128		80	102		128	
Enclosure	FFVE 1517	FFVE 1517	FFVA 1760	FFVC 1760	FFVC 1760	FFVD 1760	FFVC 1760	FFVD 1760
Number of transceivers GTH+GTY	32+20	32+24	44+32	32+16	32+16	44+28	32+16	44+28
Total number of transceivers	52	56	76	48	48	72	48	72
Example price	ca. \$3500	ca. \$4600	ca. \$7900* (\$5000 ?)	ca. \$3900	ca. \$4400	ca. \$4900	ca. \$4900	ca. \$5400

The interesting result is that the Zynq UltraScale+ chips are available at prices similar to the comparable Kintex UltraScale+ chips. Therefore it is worth to consider if the CRI design may benefit from the availability of the additional quad-core 64-bit ARM CPU.

2.3 usability of ARM in the CRI

Usability of the ARM processor in the CRI is unclear. To fully utilize its potential e.g. for data preprocessing it would be necessary to equip the board with the DDR memory, which may complicate the PCB layout and increase the cost. Additionally, such utilization of the CPU would require that the transmitted data should be transferred through the DDR memory to make them available for the CPU. However, at the DDR4 speed of 2400MT/s (according to [27]), even the 64-bit wide memory does not allow to transfer the whole data stream to and from the memory (if we consider the necessary margin resulting from the fact, that this memory will be also used as a code memory). Therefore, it seems that the ARM processor may be used only with the in-chip 1 MB L2 cache memory “bare metal” configuration for control and diagnostic purposes*.

2.4 Clocks and synchronization

The CROB modules (and further FEB boards) need precise synchronization both by delivery of dedicated clock signal as well as synchronous control commands. For this purpose, all CRI modules need to be synchronized together. There are several ways to achieve it:

- To embed clock recovery circuit and synchronization engine utilizing i.e. White Rabbit^{28,29} or other protocol on every CRI board. The clock is received from the optical signal from the SFP transceiver.
- To build a dedicated receiver board³⁰ or use standard WR node in the form of a PCIe card.³¹ Then distribute clock and timing signals using peer-to-peer or daisychain connectors, i.e. popular and low-cost miniSAS.
- To deliver both clock and control messages using dedicated optical or copper links to each CRI board from external distribution unit. For example it may be possible to reuse the TTC-PON system developed at CERN.^{32,33}

The selected FPGA chips are capable to support all the above options. However, the additional hardware resources (e.g. the clock jitter cleaner) must be included in the board design.

2.5 Requirements related to FPGA resources

The simplified analysis of the STS data^{34,35} shows, that the critical logic resource may be the BRAM blocks, that will be used for sorting of data received from the SMX2 chips. Using the simple “stream merger” approach we need a single BRAM for each connected SMX2 link.³ In the worst case, there may be up to 40 SMX2 links connected to a single CROB, resulting in the consumption of 320 BRAMs in the 8-CROB configuration and 480 BRAMs in the 12-CROB configuration. All the above chips offer significantly more BRAM blocks. Consumption of other FPGA resources will be evaluated after the creation of the prototype version of the CRI firmware, which should be possible after the GBT compatible version of the SMX2 controller is created.¹⁶ The PCIe transmission of data may be accomplished either by the modified PCIe cores from the FLIB firmware,^{9,10} or by a dedicated DMA block³⁶ based on a Xilinx XDMA IP-core.³⁷

3. COST ANALYSIS

The CRI board connected to 8 CROB boards may be implemented as a PCIe board with single PCIe 16xGen3 or 8xGen4 connector. In the case of CRI supporting 12 CROBs, if the optimistic bandwidth assessment can't be applied, it is necessary to equip board with two PCIe connectors - that may lead to the design and mechanical problems, and Flex PCB technology would have to be used in such case. However, it must be taken into consideration that due to MiniPOD or MicroPOD heatsinks it is unclear if even with a single PCIe connector, it will be possible to use all PCIe slots in the computer mainboard. The estimated cost per serviced CROB is (assuming \$130 for MicroPOD Tx and \$280 for MicroPOD Rx):

- $(2 \cdot \$280 + \$130 + \$3500) / 8CROBS \approx \524 in case of 8-CROB version with XCKU11P in FFVE1517 enclosure.
- $(3 \cdot \$280 + \$130 + \$4600) / 12CROBS \approx \464 in case of 12-CROB version with XCKU15P in FFVA1517 enclosure (optimistic assessment).

*It may also be possible to connect a slower 32-bit LPDDR memory to the SoC. That should allow using Linux for control and diagnostic purposes without significant increase of PCB complexity.

- $(3 \cdot \$280 + \$130 + \$5000) / 12CROBS \approx \498 in case of 12-CROB version with XCKU15P in FFVA1760 enclosure (pessimistic assessment).

It is worth to mention, that replacement of the Kintex UltraScale+ with the Zynq UltraScale+ does not change the cost significantly.

- $(2 \cdot \$280 + \$130 + \$3900) / 8CROBS \approx \574 in case of 8-CROB version with ZU11EG in FFVC1760 enclosure.
- $(3 \cdot \$280 + \$130 + \$4900) / 12CROBS \approx \489 in case of 12-CROB version with ZU17EG in FFVD1760 enclosure.

In the case of the 8-CROB version, it should be possible to upgrade the board by mounting the KCKU15P part instead of KCKU11P in the same package (or ZU17EG instead of ZU11EG), if the amount of resources is insufficient. Similarly in the case of Zynq-based 12-CROB version, it is possible to slightly increase the number of logical resources by replacement of ZU17EG with ZU19EG.

The visualization of a possible CRI board in a PCIe format is shown in Fig. 3.

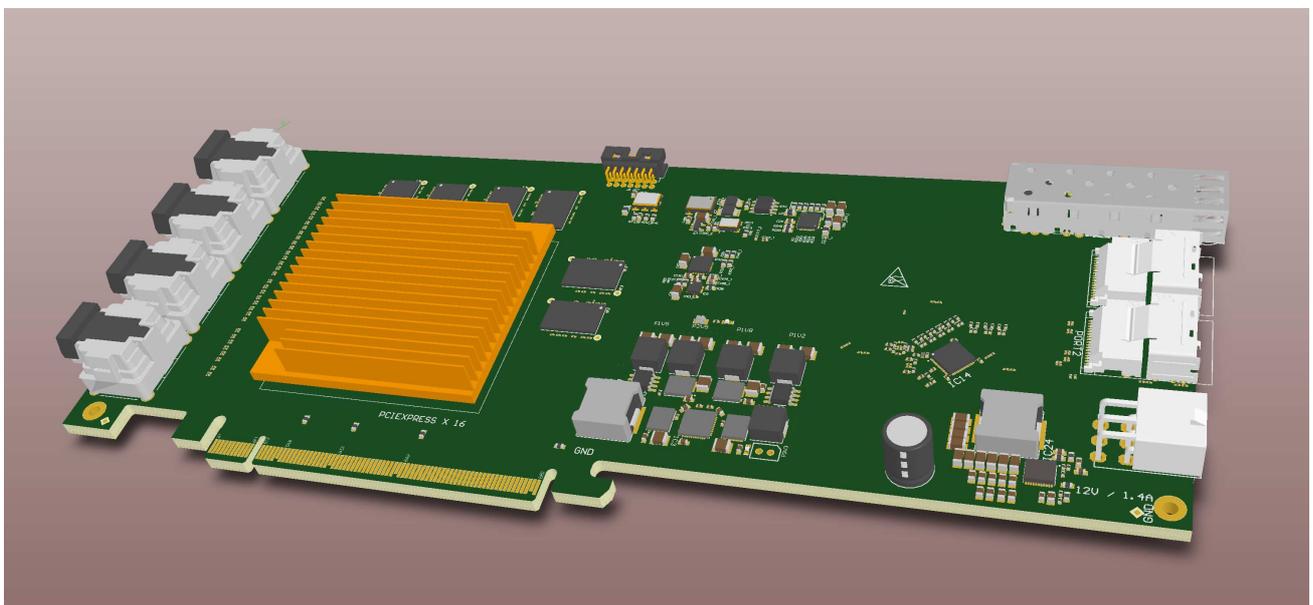


Figure 3: Visualization of a possible CRI board in the PCIe format. In the visualization, the MiniPOD transceivers have been used. The MicroPOD transceivers will be even smaller. The 12-CROB variant is shown with three Rx and one Tx MiniPODs. The SFP connector is supposed to be used for the TFC connection.

4. CONCLUSIONS

The performed preliminary analysis shows that it is possible to create the CRI board as a PCIe card, using the currently available Xilinx UltraScale+ or Zynq UltraScale+ chips. There are two possible solutions. One where a single CRI board services 8 CROB boards, and another where a single CRI board services 12 CROB boards. Both solutions seem to have a similar cost per a serviced CROB. The 12-CROB version offers slightly lower (ca. 12%) cost, but it may pose more design and technological problems (a higher number of multi-gigabit links resulting in more complex PCB routing, a higher number of optical transceivers, probably two PCIe connectors). Therefore, the 8-CROB version seems to be a safer choice. Before the final decision is taken, it is necessary to negotiate the component prices with vendors, as the prices offered for a scientific project may be lower. Additionally, it is necessary to take into consideration the computer platform in which the CRI boards will be used, and results of PCB design and implementation of the prototype firmware.

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